## EC 1354-Principles of  VLSI  Design

**UNIT I          MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY**

**PART-A**

1.  What are the four generations of integrated circuits?
2.  Give the advantages of IC.
3.  Give the variety of integrated circuits.
4.  Give the basic process for IC fabrication.
5.  What are the various silicon wafer preparations?
6.  Give different types of oxidation.
7.  What is the transistors CMOS technology provides?
8.  What are the different layers in MOS transistors?
9.  What is enhancement mode transistor?
10. What is depletion mode transistor?
11. When is the channel said to be pinched- off?
12. Give the different types of CMOS process.
13. What are the steps involved in twin-tub process?
14. What are the advantages of silicon-on-insulator process?
15. What are the advantages of CMOS process?
16. What is the fundamental goal in device modeling?
17. Define short channel devices.
18. What is pull down device?
19. What is pull up device?
20. Why NMOS technology is preferred more than PMOS technology?
21.  What are the different operating regions for an MOS transistor?
22. What are the different MOS layers?
23. What is the stick diagram?
24. What are the uses of stick diagram?
25. Give the various color coding used in stick diagram.
26. Define threshold voltage for a MOSFET?
27. What is body effect in MOSFETs?
28. How is the gate of a p channel MOSFET activated?
29. What is enhancement mode FET?
30. What specifications you will consider for selecting a MOSFET?
31. What are the requirements of a successful chip design?
32.  What are the steps performed to achieve lithography friendly design?\

# PART-B

1. Explain the operation of nMOS enhancement transistor.
2. Explain the operation of pMOS enhancement transistor.
3. Derive the threshold voltage equation of nMOS transistor with and without body effect.
4. Derive the threshold voltage equation of pMOS transistor with and without body effect.
5. Derive the MOS Dc equations of an n-channel MOSFET.
6. Derive the equation for threshold voltage of a MOS transistor and threshold voltage in terms of flat band voltage.
7. Derive expressions for the drain to source current in the non-saturated and saturated regions of operation of an nMOS transistor.

Explain the second order effects of MOSFET.

9. Define and drive the transconductane of nMOS transistor.

10. Discuss the small signal model of an nMOS transistor.

11. What is meant by channel length modulation ? Explain.

12. Explain Body effect. Explain how Body effect affects the threshold voltage.

13. Explain in detail the MOS transistor figure of merit $w_0$.

14. Explain the various features of CMOS technology.

15. Explain the IC fabrication steps with neat diagram.

16. Explain in detail the CMOS technology with neat diagram.

17. Explain the n-well CMOS process in detail.

18. Explain the p-well CMOS process in detail.

19. Explain the twin- tub process in detail.

20. Explain the SOI process in detail.

**UNIT II        INVERTERS AND LOGIC GATES**

## PART-A

1. Define threshold voltage in CMOS.
2. What is body effect?
3. Compare between CMOS and Bipolar technology.
4. What is channel-length modulation?
5. What is latch-up?
6. Give the basic inverter circuit.
7. Give the CMOS inverter DC transfer characteristics and operating regions.
8. Define rise time.
9. Define fall time.
10. Define delay time.
11. What are the two components of power dissipation?
12. Give some of the important CAD tools.
13. What are the advantages of CMOS over NMOS?
14. What is a BiCMOS?
15. What is meant by epitaxy?
16. What are the problems of BiCMOS?
17. What is CMOS standard cell characterization methodology?
18. Give CMOS process steps.
19. What are the basic processing steps involved in BiCMOS fabrication process?
20. Differentiate between channeled and channel less gate array.

## PART-B

1. Explain the encoding for a single metal MOS layer representation.

2. Explain Lambda-based design rule.
3. Differentiate Lambda-based and micron based design rule.
4. Explain the n-well CMOS design rules.
5. Draw the stick diagram and mask layer representation of CMOS Inverter, NAND and NOR gate.
6. Draw the stick diagram and mask layer representation of nMOS Inverte.
7. Explain the inverter ratio of nMOS device.
8. Explain the different configuration of nMOS inverter.
9. Derive th pull-up to pull-down ratio for an inverter    driven by another nMOS inverter.
10. Derive the pull-up to pull-down ratio for an nMOS

    inverter driven through one or more pass transistors.

11. Explain CMOS Inverter DC characteristics.

12. Explain the influence of $B_n/B_p$ in CMOS inverter DC transfer characteristics.

13. Explain Noise Margin.

14. Explain the switching characteristics of CMOS inverter.

15. Explain super buffer.

16. Derive the characteristics delay through the inverter when driving large capacitive loads.

17. Write notes on

   (a) CMOS logic

   (b) BiCMOS logic

   (c) Pseudo nMOS logic

   (d) Dynamic CMOS logic

   (e) Static CMOS logic

   (f) CMOS Domino logic

   (g) Domino – Zipper logic

   (h) Cascade Voltage Switch logic (CVSL)

   (i) Pass transistor

   (j) Transmission gates

### UNIT III    CIRCUIT CHARACTERISATION AND PERFORMANCE
ESTIMATION

# PART-A

1. What is verilog?
2. What are the various modeling used in verilog?
3. What is structural gate-level modeling?
4. What is switch-level modeling?
5. What are identifiers?
6. What are the value sets in verilog?
7. What are the types of gate arrays in ASIC?
8. Give the classifications of timing control?
9. Give the different arithmetic operators?
10. What are gate primitives?
11. Give two blocks in behavioral modeling.
12. What are the types of conditional statements?
13. Name the types of ports in verilog.
14. What are the types of procedural assignments?
15. Give CMOS transfer D.C transfer characteristics and operating regions.
16. What is latch-up?
17. What is mean by power and power dissipation?
18. What is mean by PDP?
19. What is EDP?
20. What are the two types of power dissipation? State their cases.
21. What are the measures taken in the design achieving better yield?

# PART-B

1. Derive the expression for uniform and non- uniform
   resistance of a conductor.

2. Derive the expression of resistance in three operation regions of MOS design.
3. Derive the capacitance of three operating modes of MOS
   device.

4. Derive the capacitances of three regions of operation of
   MOS device.

5. Explain the source/drain capacitance.

6. Explain the routing capacitance of MOS device.

7. Explain the fringing effects in MOS device.

8. Derive the expression for multiple conductor capacitances.

9. Explain the distributed RC effect in CMOS device.

10. Write short note on wire – length design guide.

11. Explain the determination of inductance in an IC.

12. Explain the switching characteristics of CMOS device.

13. Explain the methods of transistor sizing.

14. Explain the minimization of RC effect in CMOS inverter chain.

15. Explain the power dissipation in CMOS circuit.

16. Explain design margin in detail.

17. Explain charge sharing in detail.

18. Explain the scaling of CMOS device in detail.

**UNIT IV     VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN**

# PART-A

1. What are the different symbols for transmission gate?
2. Give the different types of ASIC.
3. What is the full custom ASIC design?
4. What is the standard cell-based ASIC design?
5. Give the constituent of I/O cell in 22V10.
6. What is a FPGA?
7. What is an antifuse?
8. What are the different levels of design abstraction at physical design?
9. What are macros?
10. What are programmable interconnects?
11. Give the steps in ASIC design flow.
12. Give the XILINX configurable logic block.
13. Give the XILINX FPGA architecture.
14. Give the different symbols for transmission gate?
15. What are the considerations while performing floor plan?
16. What does synthesis mean?
17. What are the various ways to reduce clock insertion delay in the design?
18. What is meant by virtual clock definition and why it is needed?
19. What is an electrical test?
20. Why perform an electrical test?
21. What is fault localization?
22. Why perform fault localization?
23. What is boundary scan?
24. Define BIST.
25. What are the various yield-losses in the design?
26. What are the categories of testing?
27. What are functionality tests?
28. What are manufacturing tests?
29. What are the tests for I/O integrity?
30. What is meant by fault models? Give examples.
31. What is stuck-at-fault?
32. What is meant by observability?
33. What is meant by controllability?
34. What is known as percentage-fault coverage?
35. What is the meaning of fault grading?

36. What is fault sampling?
37. How to increase the speed of fault simulation?
38. What are different methods used in design for testability?
39. Enlist different scan-based test techniques?
40. What is IDBQ testing?
41. What are the applications of chip level test techniques?
42. What is boundary scan?
43. What is the test access port?
44. What is the TAP controller?
45. What is the test data register?

# **PART-B**

1. Explain the different configuration to implement Multiplexer.

2. Explain the design of decoder circuit.
3. Explain the design of priority encoder circuit.
4. Explain the design of shift / rotate registers.
5. Explain the design of arithmetic circuits.
6. Explain the design for
    (a)    Ripple Carry Adder
    (b)    Look – Ahead Adder
    (c)    Carry- Skip Adder
    (d)    Carry select Adder
    (e)    Carry – Save Adder
7. Explain the design of array multiplier circuit.
8. Explain the design of Booth multiplier circuit.
9. Explain the design of Wallace tree multiplier circuit.
10. Explain the physical design for VLSI circuits.

11. Explain the interconnect delay modeling.

12. Explain Cross talk in detail.

13. Explain the power distribution scheme in detail.

14. Explain the clock distribution scheme in detail.

15. Explain the floor planning in detail.

16. Explain the types of Testing.

17. Explain the manufacturing test principles.

18. Explain Fault models with examples.

19. Enumerate on physical faults with examples.

20. Explain the short – circuit and open – circuit faults with example.

21. Explain the controllability and observability for digital circuit.

22. Explain the algorithms of Automatic Test – pattern generation.

23. Explain the D-calculus and PODEM algorithm with an example.

24. Explain Built-in self test.

25. Explain with diagram the IDDQ testing.

26. Explain in detail Boundary-scan testing.

**UNITV    VERILOG HARDWARE DESCRIPTION LANGUAGE**

# **PART-A**

1. Mention the levels at which testing of a chip can be done?
2. What are the categories of testing?
3. Write notes on functionality tests?
4. Write notes on manufacturing tests?
5. Give some circuit maladies to overcome the defects?
6. What are the tests for I/O integrity?
7. What is meant by fault models?
8. Give some examples of fault models.
9. What is stuck-at fault?
10. What is meant by observability?
11. What is meant by controllability?
12. What is known as percentage-fault coverage?
13. What is fault grading?
14. Mention the ideas to increase the speed of fault simulation?

15. What is fault sampling?
16. What are the approaches in design for testability?
17. Mention the common techniques involved in ad hoc testing?
18. What are scan-based test techniques?
19. What are self test techniques?
20. What is known as BILBO?
21. What is known as IDBQ testing?
22. What are the applications of chip level test techniques?
23. What is boundary scan?
24. What is the test access port?
25. What are the contents of the test architecture?
26. What is the TAP controller?
27. What is known as test data register?
28. What is known as boundary scan register?
29. What are the types of gate arrays in ASIC?
30. What are gate primitives?
31. State different levels of design abstraction at physical design.

# **PART-B**

1. Explain the typical design flow for designingVLSI IC circuits.

2. What are the advantages of HDL? Explain the major Capabilities of HDL language.

3. Explain Design methodology to implement digital circuit.
4. Explain the comiler directives of veriolog HDL.
5. Explain the system tasks and functions of verilog HDL.
6. Explain various features of gate level modeling.
7. Explain various features of switch level modeling.
8. Explain the gate delays.
9. Explain the various features of data flow modeling.
10. Explain the operators in data flow modeling.

11. Explain various features of behavioral modeling.

12. Write notes on.

(a) procedural constructs

(b) Initial statement

(c) always statemtnt

13. Write short notes on

      i.    Timing control in behavioral modeling
     ii.    Block statement

14. Write a brief note on the conditional statements available

    in verilog.

15. Write notes on

      i.    Assign – deassign statement
     ii.    Force – release statement

16. Explain the structural gate level description of 2-to-4

    decoder.

17. Explain the structural gate level description of 8-bit

    equality detector.

18. Explain the structural gate level description of 4-bit

    magnitude comparator.

19. Explain the structural gate level description of 4-bit

    priority encoder.

20. Explain the structural gate level description of full adder

    circuit.

21. Explain the structural gate level description of ripple carry

    adder.

22. Write a verilog program for 3 to 8 decoder in gate level

    description.

23. Write a verilog program for 8-bit full adder using one bit

    full adder using behavioral modeling.

24. Give a verilog structural gate level description of a bit comaparator.

25. Give a brief account of timing control and delay in verilog.

26. Explain in detail behavioral and RTL modeling.